IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	A. Bhavnagarwala et al.	**Examiner:** West, Jeffrey R.	
Serial No.:	10/643,193	**Group:** Art Unit 2857	
Filed:	August 18, 2003	**Docket:** YOR920030289US1 (8728-635)	

For: **CIRCUITS AND METHODS FOR CHARACTERIZING RANDOM VARIATIONS IN DEVICE CHARACTERISTICS IN SEMICONDUCTOR INTEGRATED CIRCUITS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

AMENDED APPEAL BRIEF

This Appeal is from a Final Office Action mailed on January 9, 2007 (hereinafter, referred to as the "Final Action"). This Appeal was commenced by a Notice of Appeal and Pre-Appeal Brief Request for Review filed on May 9, 2007, a Notice of Panel Decision mailed on June 25, 2007, and the Notice of Non-Compliant Appeal Brief dated February 27, 2008. Appellants hereby submit this Amended Appeal Brief in furtherance of the Appeal.

The Notice of Non-Compliant Appeal Brief indicated that Claims 17 and 37 were not listed in the grounds of rejection. Respectfully, the grounds for rejection do not include Claims 17 and 37. Due to the withdrawal of the rejections under 35 USC 101 in the Notice of Panel Decision from Pre-Appeal Brief Review Claims 17 and 37 are not under appeal and are believed to be allowable. In view of the foregoing, the Status of Claims has been clarified in this paper.

Appeal from Group 2857

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I. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is International Business Machines Corporation, the assignee of the entire right, title and interest in and to the subject application by virtue of an assignment of recorded in the U.S. Patent and Trademark Office.

II. RELATED APPEALS AND INTERFERENCES

There are no Appeals or Interferences known to Applicant, Applicant's representatives or the Assignee, which would directly affect or be indirectly affected by or have a bearing on the Board's decision in the pending Appeal.

III. STATUS OF CLAIMS

Claims 1, 3-13, 15-19, 26, 27, 29, and 32- 38 are pending. Claims 1, 3-13, 15, 16, 18, 19, 26, 27, 29, 32-36, and 38 stand rejected and are under appeal. Claims 2, 14, 20-25, 28 and 30-31 are canceled. Claims 17 and 37 are allowable. The claims are set forth in the attached Appendix.

IV. STATUS OF AMENDMENTS

No After Final Amendments have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the claimed inventions are directed to systems and methods for measuring and characterizing random variations in device characteristics of semiconductor integrated circuit devices. In the design of semiconductor integrated circuits, it is very important to consider variations in device characteristics (device mismatch) such as Vt (threshold voltage) for a given circuit design, in order to achieve circuit robustness and obtain high manufacturing functional yields for such devices. The claimed inventions provide methods that enable circuit designers to accurately measure and characterize random variations in device characteristics (such as transistor threshold voltage (Vt)) by obtaining and analyzing subthreshold DC voltage characteristic data (Vout vs. Vin) for transistor device pairs.

For purposes of illustration, the claimed inventions will be described with reference to certain Figures and corresponding text of Appellants' Specification, for example, but nothing herein shall be deemed as a limitation on the scope of the invention. For each Claim listed below, the claim elements are presented in italicized text, and are followed by citation to exemplary figures and/or supporting text in Appellants' Specification (Spec.).

Claim 1 recites:

A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices,

and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region;

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

Support for the subject matter of Claim 1 can be found as follows:

A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of **(see, e.g., Spec. page 16, lines 3-14; see generally, FIG. 10, page 22, lines 15 et seq.)**

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} *as a function of an input DC voltage* V_{IN}, **(see, e.g., FIGs. 5B, 7B, Spec. page 19, lines 4-18; page 20, lines 11-20; page 21, line 17 ~ page 22, lne 4)**

wherein V_{IN} *is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein* V_{OUT} *is obtained at a common node connection of the first and second semiconductor transistor devices, (***see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; **(see, e.g., Spec. page 17, lines 10 ~ page 19, line 3);**

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices. **(see, e.g., Spec. page 20, line 21 ~ page 21, line 7)**

Claim 10 recites:

A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

Support for the subject matter of Claim 10 can be found as follows:

A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of **(see, e.g., Spec. page 16, lines 3-14; see generally, FIG. 10, page 22, lines 15 et seq; FIGs. 11, 12, 13 and 14; Spec. page 24 ~ page 31).**

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3; FIGs. 11, 12, 13 and 14; Spec. page 24 ~ page 31);**

wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, **(see, e.g., FIGs. 5B, 7B, Spec. page 19, lines 4-18;, Page 20, lines 11-20; page 21, line 17~ page 22, line 4)**

wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region; **(see, e.g., Spec. page 17, lines 10 ~ page 19, line 3);**

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair; **(see, e.g., Spec. page 20, line 21 ~ page 21, line 7; FIG. 9)**

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; andcharacterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit. **(see, e.g., Spec. pp. 26 ~ 31)**

Claim 26 recites:

A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistors devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

Support for the subject matter of Claim 26 can be found as follows:

A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising: **(see, e.g., Spec. page 16, lines 3-14; see generally, FIG. 10, page 22, lines 15 et seq; page. 31, lines 5-14)**

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, **(see, e.g., FIGs. 5B, 7B, Spec. page 19, lines 4-18; page 20, lines 11-20; page 21, line 17 ~ page 22, line 4)**

*wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, (***see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; **(see, e.g., Spec. page 17, lines 10 ~ page 19, line 3);**

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices. **(see, e.g., Spec. page 20, line 21 ~ page 21, line 7)**

Claim 27 recites

A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

Support for the subject matter of Claim 27 can be found as follows:

A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising: **(see, e.g., Spec. page 16, lines 3-14; see generally, FIG. 10, page 22, lines 15 et seq; page. 31, lines 5-14)**

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3; FIGs. 11, 12, 13 and 14; Spec. pp. 24 ~ 31);**

wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, **(see, e.g., FIGs. 5B, 7B, Spec. page 19, lines 4-18; page 20, lines 11-20; page 21, line 17~ page 22, line 4)**

wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, **(see, e.g., FIGs. 2, 3 or 4 for respective device pairs 20/21, 22/23, and 24/25; and Spec. page 17, lines 10 ~ page 19, line 3);**

and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region; **(see, e.g., Spec. page 17, lines 10 ~ page 19, line 3);**

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair; **(see, e.g., Spec. page 20, line 21 ~ page 21, line 7; FIG. 9,)**

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; andcharacterizing random

variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit. **(see, e.g., Spec. pp. 26 ~ 31)**

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejections Under 35 U.S.C. § 103

i. *Claims 1, 3, 5-10, 12, 26, 27, 29 and 32 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,275,094 to Cranford in view of Conti;*

ii. *Claim 4 stands rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and in view of U.S. Patent No. 6,731,916 to Haruyama;*

iii. *Claims 13 and 33 stand rejected35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. U.S. Patent No. 5,999,043 to Zhang et al;*

iv. *Claims 11 and 34 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of Zhang and further in view of U.S. Patent No. 6,819,183 to Zhou et al.;*

v. *Claims 15, 16, 35 and 36 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.;*

vi. *Claim 18 stands rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett;* and

vii. *Claims 19 and 38 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,798,278 to Ueda.*

VII. ARGUMENTS

A. Rejections Under 35 U.S.C. § 103

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). It is well established that a *prima facie* showing of obviousness requires, in general, a two part analysis – starting with a claim interpretation analysis to determine the scope and substance of the subject matter being claimed, followed by an obvious analysis to determine whether the claimed subject matter (as interpreted) is obvious in view of the prior art. Once the claims have been properly constructed, the Examiner has the burden of establishing a *prima facie* case of obviousness. 'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

i. *Claims 1, 3, 5-10, 12, 26, 27, 29 and 32 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,275,094 to Cranford in view of Conti*

It is respectfully submitted that the obviousness rejections set forth in the Final Action, which are premised primarily on the combined teachings of Cranford and Conti, are legally deficient as a matter of law. Indeed, as will be explained below, at the very least, the obviousness rejections of Claims 1, 10, 26 and 27 are based on clear misinterpretations and mischaracterizations of the teachings of Cranford and Conti as applied to the claimed inventions, as well as an obviousness analyses that employ improper use of hindsight reasoning to

selectively pick among unrelated, disparate prior art teachings to derive the claimed subject matter with no motivation for combining the reference teachings.

With regard to Claims 1, 10, 26 and 27, Applicants contend that the combination of Cranford and Conti does not teach or fairly suggest a process for characterizing device mismatch in a semiconductor integrated circuit, comprising, for example, *obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region, and processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices*, as essentially claimed in Claims 1, 10, 26 and 27.

In formulating the obviousness rejection of claim 1, for example, the Examiner relies primarily on the teachings of Cranford as anticipating the above elements of claim 1 (see page 5 of the Final Action) and relying on Conti as teaching a test structure for threshold voltage mismatch using subthreshold DC voltage characteristic data (see page 8 of the Final Action). However, the Examiner's reliance of the teachings of Cranford and Conti in this regard is wholly misplaced

For example, on page 5 of the Final Office Action, the Examiner essentially contends that Cranford teaches *obtaining DC characteristic data for a device pair* (Col. 7, lines 4-9, Col. 8, lines 1-4) *comprising an output DC voltage as a function of an input DC voltage* (col. 7, lines 14-16) and processing the DC voltage characteristic data to determine a distribution of device mismatch (Col. 7, lines 20-23 and 28-36). The Examiner's reliance on the cited sections of Cranford in this regard is technically erroneous as a matter of fact.

Cranford teaches in the cited sections a method for dynamically generating a voltage to correct threshold mismatch between transistor devices in a differential amplifier to thereby correct for manufacturing offset (See Abstract; and Col. 7, lines 20-23). Cranford explains that this is done by performing a Fast Fourier Transform analysis to identify harmonic differences in the AC input-output signals at input and output terminals to determine mismatch between input and output harmonics where any mismatch is translated into a voltage representative of the offset between the differential transistor pair, and where the feedback voltage is returned to the differential pair to eliminate the effect of offset (see, Col. 4, lines 34-44).

Cranford teaches (in Col 7, lines 44-55 that the input signals (160) and (162) input to terminals 112 and 114 and output signals of terminals 116 and 120 are AC sinusoidal signals that are analyzed for purposes of determining threshold voltage offset (see, AC signals of FIG. 6). Moreover, Col. 8, lines 1-4 of Cranford states that:

> **FIG. 8 shows the change in various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminal 116, 120 (see FIG. 5).**

FIG. 8 is nothing more than a representation of the offset in FIG. 7 in terms of amplitude and frequency for the various harmonics in the output signal prior to correction of offset voltage (see, Col, 5, lines 4-6). In other words, FIG. 8 illustrates Amplitude (in db) of the output signal as a function of Frequency *(i.e., Output Voltage Amplitude vs. Frequency).*

In view of the above, the Examiner's assertion that Cranford teaches ***obtaining DC voltage characteristic data*** *for a device pair comprising first and second semiconductor transistor devices,* ***wherein the DC voltage characteristic data comprises an output DC voltage*** V_{OUT} ***as a function of an input DC voltage*** V_{IN}, *wherein* V_{IN} *is applied to a gate of at least one*

of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices lacks support.

At most Cranford teaches a process of determining/correcting threshold voltage offset using FFT analysis of the harmonics of AC input-output sinusoidal signals, which are clearly distinct from the claimed invention of obtaining and using DC voltage characteristic data to determine device mismatch.

The Examiner's interpretation of FIG. 8 of Cranford as disclosing **DC voltage V_{OUT} *as a function of an input DC voltage V_{IN}***, is misplaced, especially given the clear and explicit teachings of Cranford as to what FIG. 8 represents. Further, the Examiner fails to explain how a *process of correcting threshold mismatch by performing a fast Fourier transform analysis to detect harmonic differences identified by the FFT between sinusoidal input-output signals* as taught by Cranford is even remote the same or similar to the claimed process of *processing the DC voltage characteristic data* (which is *output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}) to determine a distribution of device mismatch between the first and second semiconductor transistor devices* as claimed in Claims 1 and 26, for example.
Indeed, it is clear that Cranford does not teach the use of *DC voltage characteristic data* as claimed to determine device mismatch, but rather the use of FFT analysis of AC input-output signals to determine differences in harmonics of sinusoidal input-output voltages and correlate the differences to device offset. In this regard, the Examiner's arguments as premised on Cranford are fundamentally flawed on technical and legal grounds.

In any event, on page 8 of the Final Office Action, the Examiner admits that Cranford does **not teach** obtaining DC voltage characteristic data of a transistor pair when the transistors

are operating in the sub-threshold region. In this regard, the Examiner essentially acknowledges that Cranford does not teach every feature of the claimed inventions of Claims 1, 10, 26, and 27. Instead, the Examiner relies on Conti as teaching "obtaining subthreshold DC voltage characteristic data for adjacent transistors" contending that it would be obvious to modify the teachings of Cranford to include the use of DC voltage characteristic data of a transistor pair operating in the subthreshold regime as taught by Conti

The Examiner's reliance on Conti in this regard is *grossly* misplaced on two fundamental levels. First, *Conti* teaches a mismatch model based on measurements of drain current ID (see page 173, second column on bottom). The Examiner seemingly misunderstands the *fundamental difference* between **DC Voltage characteristic data** (as claimed) and **DC Current characteristic data** (as disclosed in Conti). In fact, as presented at pages 6-9 of the Background section of Applicants' specification, there are problems associated with the use of DC Current characteristic data (as taught by Conti) for purposes of evaluating device mismatch. In this regard, Conti clearly teaches away from the claimed invention and renders the rejection legally deficient on its face.

Moreover, the Examiner takes a leap to explain motivation for modifying Cranford with Conti. Again, Cranford does not teach DC voltage characteristic data to determine device mismatch, but rather FFT analysis of AC signals. Moreover, Cranford's process of correction of mismatch is not compatible with the transistor pairs under consideration being operated in the "subthreshold regime." Cranford teaches a real-time correction process in which the transistor pairs under consideration are not biased to operate in the subthreshold regime (or the circuit would not work). The proposed combination of Conti and Cranford as applied to Claims 1, 10,

26, and 27 in this regard is not tenable for at least the above reasons. Thus, withdrawal of the rejection of Claims 1, 10 26 and 27 is respectfully requested.

Claims 3, 5-9 depend from Claim 1. Claim 12 depends from 10. Claims 29 and 32 depend from 29. The dependent claims are believed to be allowable for at lease the reasons given for the respective independent claims.

ii. *Claim 4 stands rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and in view of U.S. Patent No. 6,731,916 to Haruyama*

Claim 4 depends from Claim 1 and is believed to be allowable for at least the reasons given for Claim 1. Withdrawal of the rejection is respectfully requested.

iii. *Claims 13 and 33 stand rejected35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. U.S. Patent No. 5,999,043 to Zhang et al*

Claim 13 depends from Claim 10. Claim 33 depends from Claim 27. The dependent claims are believed to be allowable for at least the reasons given for Claims 10 and 27, respectively. Withdrawal of the rejection is respectfully requested.

iv. *Claims 11 and 34 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of Zhang and further in view of U.S. Patent No. 6,819,183 to Zhou et al.*

Claim 14 depends from Claim 10. Claim 34 depends from Claim 27. The dependent claims are believed to be allowable for at least the reasons given for Claims 10 and 27,

respectively. Withdrawal of the rejection is respectfully requested.

v. *Claims 15, 16, 35 and 36 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al*

Claims 15 and 16 depend from Claim 10. Claims 35 and 36 depend from Claim 27. The dependent claims are believed to be allowable for at least the reasons given for Claims 10 and 27, respectively. Withdrawal of the rejection is respectfully requested.

vi. *Claim 18 stands rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett*

Claim 18 depends from Claim 10 and is believed to be allowable for at least the reasons given for Claim 10. Withdrawal of the rejection is respectfully requested.

vii. *Claims 19 and 38 stand rejected 35 U.S.C. § 103 as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,798,278 to Ueda*

Claim 19 depends from Claim 10. Claim 38 depends from Claim 27. The dependent claims are believed to be allowable for at least the reasons given for Claims 10 and 27, respectively. Withdrawal of the rejection is respectfully requested.

viii. Conclusion

Each of the 103 rejections is based on the primary combination of Cranford and Conti as applied to Claims 1, 10, 26 and 27, therefore, the rejections are believed to be legally defective for at least the reasons given above for Claims 1, 10, 26 and 27. Indeed, the dependent claims are believed to be allowable for at least the reasons given for Claims 1, 10, 26 and 27. Accordingly, withdrawal of the obviousness rejections is respectfully requested.

Accordingly, for at least the above reasons, it is respectfully requested that the Board reverse all claim rejections under 35 U.S.C. §103.

Respectfully submitted,

Dated: March 28, 2008

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VIII. Claims Appendix

1. A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

3. The method of claim 1, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

4. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises retrieving said DC voltage characteristic data from a database.

5. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises measuring subthreshold DC voltage characteristic data in a subthreshold region of the transistors.

6. The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

7. The method of claim 1, further comprising the step of determining a variation in a device characteristic for a device of the integrated circuit comprising the device pair.

8. The method of claim 7, further comprising the step of assessing random variation of device mismatch of the semiconductor integrated circuit using variations in the device characteristic for each device of the integrated circuit as determined from distributions of variation of device mismatch for device pairs within the integrated circuit.

9. The method of claim 8, wherein the device characteristic comprises threshold voltage.

10. A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

11. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprises applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

12. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

13. The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises:

varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

15. The method of claim 10, wherein the step of determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprises the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN}.

16. The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of Vt mismatch between the first and second transistors when the first and second transistors each comprise an NFET.

17. The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

18. The method of claim 10, wherein the integrated circuit comprises an SRAM (static random access memory) cell.

19. The method of claim 10, wherein the step of determining a Vt variation of transistors in the integrated circuit comprises determining a standard deviation of Vt variation of the transistors.

26. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistors devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

27. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

29. The program storage device of claim 27, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

32. The program storage device of claim 27, wherein the instructions for performing the step of obtaining DC voltage characteristic data for a selected device pair comprise instructions for separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

33. The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair comprise instructions for performing the steps of:

varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

34. The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprise instructions for performing the steps of:

applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

35. The program storage device of claim 27, wherein the instructions for determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprise instructions for performing the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN}.

36. The program storage device of claim 35, wherein the distribution of V_{IN} corresponds to a distribution of Vt mismatch between the first and second transistors when the first and second transistors each comprise an NFET.

37. The program storage device of claim 35, wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

38. The program storage device of claim 27, wherein the instructions for determining a Vt variation of transistors in the integrated circuit comprise instructions for determining a standard deviation of Vt variation of the transistors.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.